REMARKS

Claims 8 -13 are pending and under consideration. Claims 1-7 stand withdrawn due to a prior election requirement.

In the Office Action, Claims 8-13 were rejected.

With this Amendment, Claim 1 was amended. No new matter was introduced as a result of this amendment.

Accordingly, claims 8-13 are at issue.

I. 35 U.S.C. § 102 Anticipation Rejection of Claims

Claims 8-12 were rejected under 35 U.S.C. § 102(e) as being anticipated by Ha et al. ("Ha") (U.S. Publication No. 2002/0072182). Although Applicant respectfully traverses this rejection, Claim 8 has been amended to clarify the invention and remove any ambiguities that may have been the basis for this rejection.

Claim 1 is directed to a semiconductor device, which comprises a semiconductor substrate, a plurality of electronic circuit elements formed at parts of the semiconductor substrate for each electrically independent region and including insulating films and electrodes formed on the insulating films.

Amended Claim 1 recites that "the insulating films differing in required electrical effective thickness for each electronic circuit element, and the electrodes having different concentrations of impurities for each circuit element with the same conductivity type according to the effective thickness." Thus, for circuit elements with the same conductivity type, their corresponding electrodes have different concentrations of impurities according to the electrical effective thickness of their associated insulating films.

In contrast, Ha states that:

> "Referring to FIG. 4, plasma doping mask is removed and gate patterns 130 and 131 and gate insulation patterns 110 are formed over an entire surface of the substrate 10 by patterning the polycrystalline silicon layer. Here, the patterning is performed using a conventional photolithography and etching process. Thus, pure polycrystalline silicon gate patterns 130 are formed in the

NMOS transistor region and polycrystalline silicon germanium gate patterns 131, so to speak, polycrystalline silicon gate patterns containing germanium are formed in the PMOS transistor region"

(See Paragraph [0035]), and moreover, Ha states that:

> "Referring to FIG. 5, sidewall spacers 17 and 19 are formed on the sidewalls of gate patterns 130 and 131, respectively. Then, ion implantation mask 140 to cover the NMOS transistor region is formed on the substrate 10 having gate patterns 130 and 131 using a conventional photolithography process and deep implantation of boron ion to PMOS transistor region is carried out to form a deeply doped source/drain region 143."

(See paragraph [0037]), and that:

> "Referring to FIG. 6, the ion implantation mask to cover the NMOS transistor region is removed. Then, other ion implantation mask 150 to cover the PMOS transistor region is formed on the substrate 10 having gate patterns 130 and 131 using a conventional photolithography process and high dose, deep implantation of N type impurity ion containing phosphor or arsenic element to NMOS transistor region is carried out to form a deeply doped source/drain region 145."

(See paragraph [0038]). Thus, Ha solely discusses doping of circuit elements with different conductivity types. Hence, Ha fails to teach or suggest "electrodes having different concentrations of impurities for each circuit element with the same conductivity type according to the effective thickness."

Hence, Claim 1 is allowable over Ha, as are dependent Claims 9 – 12, for at least the same reasons. Accordingly, Applicant respectfully requests that the claim rejections under 35 U.S.C. § 102 be withdrawn.

II. 35 U.S.C. § 103 Obviousness Rejection of Claims

Claims 8-11 and 13 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Yoshiyama et al. ("Yoshiyama") (U.S. Patent Publication No.: 2003/0151099 A1) in view of Branak et al ("Branak") (U.S. Patent Publication No.: 2003/0146479 A1). Applicant respectfully traverses this rejection, and submits that Yoshiyama and Branak may not properly be combined to reject Claim 8.

The Examiner states that Yoshiyama fails to disclose the electrodes having different concentrations of impurities, whereas Branak does disclose the doping to modify the polysilicone work function.

However, Branak discloses that:

> "The structure of complementary FETs in accordance with the present invention are shown in FIG. 2. In the illustrative embodiment, an n-channel FET 202 has a tantalum gate electrode 204 and a p-channel FET 220 has a tantalum nitride gate electrode 222. In most other respects, these transistors are similar to conventional FETs."

See paragraph [0033], and that:

> "An example of the structure of conventional FETs is shown in FIG. 1. Referring to FIG. 1, an NFET 102 includes an n-doped polysilicon gate electrode 104, source/drain regions (also referred to as terminals) 106, and gate insulator 108. The top surface of source/drain regions 106, as well the top surface of gate electrode 104 are silicided to reduce electrical resistance. Sidewall spacers 110 are adjacent to gate electrode 104. Similarly, a PFET 120 includes an p-doped polysilicon gate electrode 122, source/drain regions (also referred to as terminals) 124, and gate insulator 108. The top surface of source/drain regions 124, as well the top surface of gate electrode 122 are silicided to reduce electrical resistance. Sidewall spacers 110 are adjacent to gate electrode 122. FETs 102, 120 are isolated from other devices in an integrated circuit by shallow trench isolation structures 116."

See paragraph [0027]. Thus, Branak solely discusses doping of circuit elements with different conductivity types. Hence, Branak fails to teach or suggest "electrodes having different concentrations of impurities for each circuit element with the same conductivity type according to the effective thickness."

Hence, Claim 1 is allowable over Yoshiyama in view of Branak, as are dependent Claims 9 – 11 and 13, for at least the same reasons. Accordingly, Applicant respectfully requests that the claim rejections under 35 U.S.C. § 103 be withdrawn.

III. Conclusion

In view of the above amendments and remarks, Applicant submits that Claims 8 – 13 are clearly allowable over the cited prior art, and respectfully requests early and favorable notification to that effect.

Respectfully submitted,

Dated: April 10, 2006

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